Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Previously Presented) An analog to digital converter (ADC) comprising:

a first amplifier tracking an input voltage with its output;

a coarse ADC amplifier connected to a coarse capacitor at its input and having a coarse ADC reset switch controlled by a first clock phase;

a fine ADC amplifier connected to a fine capacitor at its input and having a fine ADC reset switch controlled by a second clock phase, wherein a set of reference voltages is selected for use by the fine ADC amplifier based on an output of the coarse ADC amplifier,

wherein the coarse capacitor is charged to a coarse reference voltage during the first clock phase and connected to the first amplifier's output voltage during the second clock phase, and

wherein the fine capacitor is connected to a fine reference voltage during the first clock phase and charged to the first amplifier's output voltage during the second clock phase; and

an encoder that converts outputs of the coarse and fine ADC amplifiers to a digital output.

2. (Original) The analog to digital converter of claim 1, wherein the coarse ADC reset switch is a field effect transistor (FET).

3. (Original) The analog to digital converter of claim 1, wherein the first and second clock phases are non-overlapping.

4. (Original) The analog to digital converter of claim 1, wherein the fine ADC amplifier includes a plurality of cascaded amplifier stages.

5. (Original) The analog to digital converter of claim 1, wherein the coarse ADC amplifier includes a plurality of cascaded amplifier stages.

6. (Previously Presented) The analog to digital converter of claim 1, wherein the coarse capacitor is connected to the first amplifier's output on a delayed second phase.

7. (Previously Presented) The analog to digital converter of claim 1, wherein the fine ADC capacitor is connected to the first amplifier's output on a delayed second clock phase and to the fine reference voltage during a delayed first clock phase.

8. (Previously Presented) The analog to digital converter of claim 1, further including a switch that connects an output of the first amplifier to the coarse capacitor on the second clock phase.

9. (Original) The analog to digital converter of claim 1, further including a coarse comparator that latches the output of the coarse ADC amplifier and outputs it to the encoder.

10. (Original) The analog to digital converter of claim 1, further including a fine comparator that latches the output of the fine ADC amplifier and outputs it to the encoder.

11. (Previously Presented) An analog to digital converter comprising:

a track-and-hold amplifier tracking an input voltage;

a first plurality of amplifiers each connected to a corresponding capacitor at its input, wherein the amplifiers of the first plurality are reset on a clock phase N_1 and their corresponding capacitors are connected to an output of the track-and-hold on a clock phase N_2;

a second plurality of amplifiers each connected to a corresponding capacitor at its input, wherein the amplifiers of the second plurality are reset on the clock phase N_2 and their corresponding capacitors are charged to the track-and-hold amplifier output voltage on the clock phase N_2 and wherein a set of reference voltages is selected based on outputs of the first plurality of amplifiers, for input to the second plurality of amplifiers on the clock phase N_1; and

an encoder that converts outputs of the first and second pluralities of amplifiers to a digital output.

12. (Previously Presented) The analog to digital converter of claim 11, further including FET switches that reset the first plurality of amplifiers on the clock phase N_1.

13. (Previously Presented) The analog to digital converter of claim 11, wherein the clock phases N_1 and N_2 are non-overlapping.

14. (Previously Presented) The analog to digital converter of claim 11, wherein each of the second plurality of amplifiers includes a plurality of cascaded amplifier stages.

15. (Previously Presented) The analog to digital converter of claim 11, wherein each of the first plurality of amplifiers includes a plurality of cascaded amplifier stages.

16. (Previously Presented) The analog to digital converter of claim 11, wherein the capacitors of the first plurality of amplifiers are connected to the track-and-hold amplifier output on a delayed clock phase N_2.

17. (Previously Presented) The analog to digital converter of claim 11, wherein the capacitors of the second plurality of amplifiers are connected to the track-

and-hold amplifier output on a delayed clock phase N_2, and to the set of reference voltages on a delayed clock phase N_1.

18. (Previously Presented) The analog to digital converter of claim 11, further including switches that connect an output of the track-and-hold to the capacitors of the first plurality of amplifiers on the clock phase N_2.

19. (Previously Presented) The analog to digital converter of claim 11, further including a first plurality of comparators that latch the outputs of the first plurality of amplifiers and output them to the encoder.

20. (Previously Presented) The analog to digital converter of claim 19, further including a second plurality of comparators that latch the outputs of the second plurality of amplifiers and output them to the encoder.

21. - 31. (Cancelled)

32. (Previously Presented) An analog to digital converter comprising:

a track-and-hold amplifier tracking an input voltage;

a first amplifier that resets on a clock phase N_1 and amplifies a difference of an output of the track-and-hold amplifier and a first voltage reference on a clock phase N_2, wherein the track-and-hold amplifier is in a hold-mode on the clock phase N_2;

a second amplifier that resets on the clock phase N_2 and amplifies a difference of the output of the track-and-hold amplifier and a second reference voltage on the clock phase N_1, wherein a first set of reference voltages is selected for use by the second amplifier based on an output of the first amplifier; and

an encoder that converts outputs of the first and second amplifiers to a digital output.

33. (Cancelled)

34. (Cancelled)

35. (Previously Presented) The analog to digital converter of claim 1, wherein the first amplifier is in a hold-mode during the second clock phase.

36. (Previously Presented) The analog to digital converter of claim 1, further including a switch matrix to select the set of reference voltages for use by the fine ADC amplifier.

37. (Previously Presented) The analog to digital converter of claim 11, wherein the track-and-hold amplifier is in a hold-mode on the clock phase N_2.

38. (Previously Presented) The analog to digital converter of claim 11, further including a switch matrix to select the set of reference voltages based on the outputs of the first plurality of amplifiers.

39. (Previously Presented) The analog to digital converter of claim 32, wherein the track-and-hold amplifier is in a hold-mode during the clock phase N_2.

40. (Previously Presented) The analog to digital converter of claim 32, further including a switch matrix to select the set of reference voltages for use by the second amplifier.